CLAIMS

What is claimed is:

1. In a digital processor, a method for temporarily halting execution of a given stream of program instructions while a processor is waiting for a subject event to occur, comprising:

in response to waiting, arming an event monitor for monitoring occurrence of events, including identifying at least the subject event; and

halting execution of the given stream of program instructions until occurrence of any one of the identified events is observed by the event monitor, said halting execution including:

monitoring, by the event monitor, for an identified event; and

upon the event monitor observing occurrence of an identified event, resuming execution of the given stream of program instructions.

2. A digital processor system for temporarily halting execution of a given stream of program instructions while a processor is waiting for a subject event to occur, comprising:

an event monitor which in response to processor waiting is armed via identification of the subject event; and

an execution scheduler, responsive to the event monitor, which, upon a request that the given stream of program instructions be halted until the subject event is observed by the event monitor, halts execution of the given stream if the subject event has not yet occurred since the event monitor was armed, and which resumes execution of the given stream upon observation of the subject event by the event monitor.

3. In a digital processing system, a system for temporarily halting execution of a given stream of program instructions while a processor is waiting for a subject event to occur, comprising:

event monitoring means;

arming means responsive to a processor waiting, the arming means arming the event monitoring means by identification of the subject event;

requesting means for requesting that the given stream of program instructions be halted until the subject event is observed by the event monitoring means; and

halting means for halting the given stream of program instructions in response to the requesting means, wherein if execution of the given stream of program instructions is halted, execution of the given stream of program instructions is resumed subsequent to observation of the subject event by the event monitoring means.

4. An electronic circuit for temporarily halting execution of a given stream of program instructions in a digital processing system while a processor is waiting for a subject event to occur, comprising:

an event monitor circuit, for monitoring for the subject event identified in response to processor waiting;

a quiesce logic circuit, which, responsive to the event monitor circuit and to a request to quiesce, temporarily halts execution of the given stream of program instructions, and which, responsive to the event monitor circuit observing occurrence of the subject event, resumes execution of the temporarily halted given stream of program instructions.

5. The method of Claim 1 wherein the step of identifying comprises identifying at least one memory location to be monitored by the event monitor, and wherein the subject event includes a modification to any such identified memory location.

6. The method of Claim 5 wherein the modification comprises a change of state.

7. The method of Claim 6 wherein a change of state includes a change of access state.

8. The method of Claim 7 wherein a change of access state is from shared to exclusive.

9. The method of Claim 7 wherein a change of access state is observed by monitoring an inter-CPU messaging bus.

10. The method of Claim 6 wherein a change of state comprises a change of value.

11. The method of Claim 10, wherein a change in value is observed by monitoring a memory bus.

12. The method of Claim 10 wherein a change in value is observed as a write to the memory location.

13. The method of Claim 1, wherein halting execution of the given stream of program instructions allows other executing program instructions to utilize available resources.

14. The system of Claim 2 wherein the subject event is identified by at least one memory location to be monitored, and wherein the subject event comprises a modification to one of the identified memory locations.

15. The system of Claim 14 wherein the modification comprises one of a change of state, a change of access state and a change of value.

16. The system of Claim 15 wherein a change in value is observed as a write to the memory location.

17. The system of Claim 14, wherein the subject event includes a write operation to one of the identified memory locations, as observed by monitoring the address on a memory write bus.

18. The system of Claim 2 wherein instructions are executed out of order.

19. The circuit of Claim 4 wherein instructions are executed out of order.

5